polysilicon fill 250 forms the three-sided gate region 200 out of silicon overlying the silicon island 122. The polysilicon deposition may be in-situ doped with a desired impurity concentration to form the three sided gate structure 200 surrounding island 122.

A2

In the Abstract:

Please replace the Abstract, page 20 lines 1-19, with the new paragraph as shown below. A marked up copy of the amended abstract illustrating the changes are shown in the Appendix to this Response.

A3

A self-aligned transistor and method making a self-aligned transistor, the transistor including a first silicon portion on an isolation layer, the silicon portion having formed therein a source region and a drain region separated by a channel region. The channel region has a first side and a second side and a top portion, and a gate oxide surrounds the channel on said first side, second side and top portion. A first, a second and a third silicon gate regions are positioned in a second silicon portion surrounding the first silicon portion about the first side, second side and top portion and the channel region.

In the Claims:

Please replace claims 17-19 as shown below. All pending claims are reproduced below, including those that remain unchanged. Marked up copies of the amended claims illustrating the changes are shown in the Appendix to this Response.

13. A method for manufacturing a dual gate transistor device, comprising:

(a) providing a substrate having silicon region and a buried oxide region formed therein;

(b) depositing a first nitride mask layer having a pattern overlying said silicon region;

(c) forming a trench in said substrate with a depth to said buried oxide;

(d) depositing a conformal oxide in said trench;

(e) forming vias in said conformal oxide adjacent to said silicon region and removing a portion of said first nitride mask to expose a portion of said silicon region;

(f) depositing polysilicon in said vias and on said portion of said silicon region; and

(g) implanting an impurity into exposed portions of polysilicon in said trench and of said silicon-on-insulator substrate underlying said second nitride layer.

14. The method of claim 13 wherein said step (c) is performed by: depositing a nitride mask layer; forming a trench window in said nitride mask layer; and etching said substrate to expose said buried oxide.

15. The method of claim 13 wherein said step (d) is performed by:
depositing a TEOS layer to fill the trench to a level equivalent to said first nitride mask layer.

16. The method of claim 13 wherein said step (e) comprises: depositing a gate layer; and
etching the vias and the first nitride layer through an opening formed in said gate layer.

17. (Amended) The method of claim 13 wherein said step (f) comprises implanting arsenic at an energy of 15-20 KeV with a zero degree tilt to provide a concentration of 2-4x10^{15}/cm^3.

18. (Amended) The method of claim 13 wherein said step (f) comprises depositing phosphorous at an energy of 7-10 KeV with a zero degree tilt to provide a concentration of the impurity in a range of 2-4x10^{15}/cm^3.

19. (Amended) The method of claim 13 wherein said step (f) comprises depositing boron at an energy of 1.5-2.5 KeV with a zero degree tilt to provide a concentration of the impurity in a range of 2-3x10^{15}/cm^3.

20. The method of claim 13 further including the step, between steps (f) and (g), of:
polishing the polysilicon and substrate.